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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,516	01/15/2004	Craig Hansen	43876-155	4560

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,516	HANSEN ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8,10-17,19-23,26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen (patent No. 5,751,614) in view of Deip (article entitled Performance Evaluation of the PowerPC 620 Microarchitecture.

3. Cohen taught the invention substantially as claimed including a data processing ("DP") system comprising (as to claims 1,10,19,26):

a) Programmable processor (PowerPC) (e.g., see col. 2, lines 1-23 and col. 5, lines 23-32);

b) Instruction path (e.g., see col. 7,lines 33-49).

c) Data path (e.g., see figs. 3,4,5,6) and col. 7,lines 12-59);

d) Execution unit coupled to the data path and operable to decode (e.g., see col. 7,lines 33-49) and executed instructions received wherein in response to decoding a single instruction specifying both a mask [MB,ME] and a register containing a data (rS) , the mask comprising fields that each correspond to a field of the data contained in the register(e.g., see fig. 3, the execution unit operable to detect some of the fields of the mask as having a predetermined value and identifying corresponding fields contained in the register as write-enabled field [fields enabled by the "1s" in the mask in figure 3];

and cause the write-enabled data field to be written to a specified register location (rA) (e.g., see fig.3). As to the writing of the write enabled data to memory, since the Power PC provided for storing of data to cache as taught by Delp on page 173, it would have been obvious to one of ordinary skill that after the data was written to the cache would have been updated to include the register data in at least one implementation of the Cohen and Delp teachings at least to provide reuse of registers.

4. Cohen did not expressly detail (claims 1, 10,19,26) an external interface. Deip however taught the PowerPC was an advanced for use with desktop systems (e.g., see page 163 col. 2 under section 2.1). Deip also taught accessing external memory via load/store instructions and interfacing using store queue. (e.g., see page 172-173 under section 7.2 cache effects). Deip also taught the PowerPC comprised instruction path and data path and execution units (e.g., see fig. 1 on page 164). Consequently one of ordinary skill would have been motivated to include an external interface at least to interface the PowerPC processor to external memory that would have store instructions and data that were not being used at a particular time by the processor as was well known in the art with respect to desktop systems.

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Cohen and Deip. Both references were direct to processing data using a PowerPC Risc processor. One of ordinary skill would have been motivated to incorporate the Deip teachings of the architecture of the PowerPC at least because the Cohen taught the system comprising a PowerPC type Risc processor and the particulars of the PowerPC processor would have allowed the one of ordinary skill to

optimized the performance of the instruction processing of Cohen at least using bypass techniques to access data in memory as taught by Deip (on page 173).

6. As to the further limitations of claim 10, Delp taught the use of the system in a desktop system, Well known desktop systems at the time of the claimed invention comprised external memory (e.g., disk memory) and a system bus to connect the components of the desktop system (such as bus to connect memory card, graphic card and motherboard etc.). Therefore one of ordinary skill would have been motivated to implement the Cohen and Deip teachings as a desktop system with an external interface for external devices including external memory (e.g., see col. 1, page 163 of Delp).

7. As to claim 2,8,11,17,20,21, 22,27,28,29, Cohen taught each of the fields of the mask has width of one bit (the "1s" in the mask where each "1" selectively indicates if a corresponding bit in the source register is to be masked) (e.g., see fig. 3 and col. 5,lines 23-62)[this controls whether the destination value is changed or not depending on the value of the mask clearly for positive logic the logic "1" and the logic inverse of would have had to have been a "0" which would provide masking of the data or not allowing data to proceed to destination].

8. As per claim 3,12 Cohen taught each of the fields of the data in the register has width of one bit (each bit in the register can be individually masked depending on the ("1s") in the mask (e.g., see fig. 3 and col. 5, lines 23-62).

9. As per claim 4,13 Cohen taught the execution unit is operable to cause the write-enabled data fields to be written to the specified memory location by reading the

unaltered field from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory locations (e.g., see fig. 3 and col. 5, lines 23-62).

10. As to claim 5,14 the mask (MB, ME)(e.g., see fig. 3) is included in the instruction and as well known in the art the instruction in the PowerPC would have been stored in a register specified at least by the program counter.

11. As to claim 6,15 also since Cohen taught the location of where the resultant data is stored is contained in the instruction (e.g., see fig. 3) and the instruction would have been stored in an instruction register in the PowerPC then the memory location would have been stored in a register.

12. As per claim 7,16,23,30 Delp taught the specified memory location comprises a section of memory having a specific and beginning at a specific memory address[(on page 173). The updated cache would have stored the data and a cache was well known to be comprise blocks of data that start at a specific location and has a specific width (width of a cache line).

13. Claim 9,18,24,25,31,32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen (patent No. 5,751,614) in view of Deip as applied to claims 1-8,10-17 above, and further in view of Kabir (patent No. 6,538,657).

14. As per claim 9,18,25,32 Kabir taught specifying plural register (corresponding to a third and fourth register when used with the instruction of Cohen) each containing a plurality of operands, multiply the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products and

provide the plurality of products to partitioned fields of a result register as a second concatenated result (e.g., see figs. 4,5a,5b) [the method of Cohen for bitwise inserting bits this allows for the Kabir system to bitwise insert data into register for processing operands where the result is stored in a second partitioned register].

15. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Cohen and Kabir. Both references were directed to toward the problems of selection of subsets of operand data and processing the data according to the partitioned subsets. One of ordinary skill would have been motivated to incorporated the Kabir teachings of partitioned multiply and concatenating the result (e.g., see figs. 4,5a,5b) at least to provide the functionality to implement the application of processing pixel data (e.g., see col. 1, lines 13-col. 2, line 17 of Kabir).

As to the further limitation of claim 24, 31, Cohen taught 64 bit processor for performing 64 bit operations. Therefore one of ordinary skill implementing the Kaibir teachings would have been motivated to incorporate 64 bit operands to take advantage of the width of registers in a more advanced 64 bit processor (e.g., see col. 10,, lines 40-56).

Response to Arguments

Applicant's arguments filed 11/15/06 have been fully considered but they are not persuasive.

The applicant argues that the priority for the instant application includes the '840 patent (and its appendix). The Examiner has reviewed the '840 patent and the (appendix to the '599 patent which is linked the '840 patent by a dependency chain that comprises a continuation in part). The Examiner contends that the operation of the '599

patent performs transferring portions of register via a data path that is narrower than the register used by the instruction execution means. The portions of the operand are stored into the register and an operation is performed on the data. However the masking or bitwise insertion operation is not taught and no means for a single instruction to perform this complex operation is taught by the '599 or '840 patents. Also the use of masking bit means is in neither patent teachings where the '599 and 840 patent merely sequentially store data in a register from a data path. The is no masking means to selectively separately determine whether one bit or bits is to be inserted while other means are used to determine whether the other bits of destination receive bit or bits. Therefore there is no support for the masking or bitwise insert operation. Without any teachings for bitwise insert or masking means the storing is merely conventional storing such as shifting in data into a memory location. The parent patents do not even provide bit lines so direct storage of data to a portion of the destination this is further evidence there could not be any means to selectively inhibit or allow storing individual bit or bits to the location where the bit or bits are intended to be stored. Consequently the other features claimed are not taught or supported by the '840 or 599 patents. As to the appendices the Examiner as reviewed the portions indicated in the applicant's remarks and cannot find support for the features claimed. Therefore the Examiner concludes that the priority for the claimed invention does not extend to the '599 or the '840 patents.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER